In the claims:

1. (Currently Amended) A method, comprising:

detecting that a processor is overheated; ~~and~~

A1 asserting a thermal trip signal from the processor;

causing the processor to enter a halt state; and

automatically removing power from the processor.

2. (Original) The method of claim 1, further comprising rebooting a computer system, the computer system including the processor.

3. (Original) The method of claim 2, further comprising throttling the processor following the reboot.

4. (Original) The method of claim 2, further comprising applying a reduced voltage to the processor during and subsequent to the reboot.

5. (Original) The method of claim 3, wherein rebooting the computer system includes rebooting the computer system after a predetermined period of time following the detection of the overheated condition.

6. (Original) The method of claim 3, wherein rebooting the computer system includes rebooting the computer system after the processor has cooled to a predetermined temperature.

7. (Original) The method of claim 3, further comprising:

detecting for a second time that the processor is overheated;

automatically removing power from the processor for a second time; and

again rebooting the computer system.

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8. (Original) An apparatus, comprising:

a processor interface unit to monitor a thermal trip signal from a processor; and

a voltage regulator module interface to assert a power off signal to a voltage regulator module in response to an assertion of the thermal trip signal.

9. (Original) The apparatus of claim 8, wherein the processor interface periodically asserts a stop clock signal to the processor in response to a system reboot following the assertion of the thermal trip signal.

10. (Original) The apparatus of claim 9, further including a status bit that is set in response to the assertion of the thermal trip signal, the status bit to indicate that the system reboot is in response to the assertion of the thermal trip signal.

11. (Original) A system, comprising:

a processor including a thermal trip signal output that is asserted in response to an overheat condition;

a power management device to receive the thermal trip signal, the power management device to assert a power off signal in response to an assertion of the thermal trip signal; and

a power supply device to deliver power to the processor, the power supply device to receive the power off signal and to cease to deliver power to the processor in response to an assertion of the power off signal.

12. (Original) The system of claim 11, wherein the power supply device is a voltage regulator module.

13. (Original) The system of claim 11, further comprising reset logic to cause a system reset in response to the assertion of the thermal trip signal.

14. (Original) The system of claim 13, the reset logic to cause the system reset in response to the assertion of the thermal trip signal after a predetermined period of time had elapsed following the assertion of the thermal trip signal.

15. (Original) The system of claim 13, the reset logic to cause the system reset in response to the assertion of the thermal trip signal after the processor has cooled to a predetermined temperature.

16. (Original) The system of claim 14, the power management device to periodically assert a stop clock signal to the processor during and following the system reset.